REMARKS

I. MPEP 714.03

In the Office Action, the Examiner contends that Applicants' previous Amendment Letter failed to comply with the provisions of MPEP 714.03. The Examiner contends that Applicants failed to address the rejections of claims 10 and 18 over Kinsman, Fukui, and Jones; claim 11 over Kinsman, Fukui and Lo; and claims 1 and 10 over Kinsman and Lo. Applicants appreciate the Examiner pointing out this oversight. All claim rejections will be addressed in this Amendment Letter.

I. Claims Rejection Under 35 U.S.C. §102(e)

In the Office Action, the Examiner has rejected Claims 27-31 under 35 U.S.C. § 102(e) as allegedly being anticipated by Shin, U.S. Patent 6,798,049. Applicants respectfully disagree with the Examiner's conclusions.

In claim 27, Applicants claim:

> A semiconductor package, comprising:
> a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof;
> a solder mask formed on the first and second surfaces of the substrate, the solder mask covering the electrically conductive patterns;
> a thin conductive film placed over the aperture and coupled to the solder mask on the first surface of the substrate, the conductive film coupled to the electrically conductive patterns on the first surface of the resin layer through openings formed in the

solder mask;

a first semiconductor chip having a first surface coupled to the thin conductive film and a second surfaces having a plurality of input/output pads formed thereon;

a second semiconductor chip having a first surface coupled to the first semiconductor chip and a second surface having a plurality of input/output pads formed thereon; and

an encapsulate for encapsulating the aperture and the first and second semiconductor chips.

In contrast, Shin discloses an adhesive layer 34 and not a conductive thin film. The adhesive layer disclosed in Shin is used as an insulator. The Examiner claims that an adhesive layer is inherently conductive because it is comprised of matter and that matter inherently conducts physical forces, and electromagnetic, thermal, and sound energy. Applicant respectfully disagrees with this overly broad statement. An insulator by definition is nonconductor of sound, heat or electricity. Shin specifically states in Column 11, lines 45-50, that the adhesive is heat resistant. Thus, Shin does not disclose the adhesive to be thermally conductive.

However, to further distinguish Applicants' claimed invention from the cited prior art, Applicants' conductive thin film extends:

> across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

In contrast, the adhesive layer 18 in Shin is coupled to the "upper surface of the opening 16 to close the opening 16..." (Column 11, lines 45-46). The Examiner contends that the adhesive layer 18 is coupled "at least indirectly physically" to the solder mask 15 and 17. Applicant is unclear on what the Examiner means by "at least indirectly physically". First, as is clearly shown in Figure 4A, the adhesive layer 18 is not coupled to the cover coat 15. Second, element 17 in Shin is not solder mask. Element 17 is a ring dam. The ring dam 17 is formed on the upper surface of the circuit board to prevent the bonding agent from contaminating the bond fingers 12. Even assuming that the ring dam 17 is a solder mask as claimed by the Examiner, no where in Shin is it disclosed or anticipated that the ring dam 17 is used for covering the electrically conductive patterns. Furthermore, no where in Shin is it disclosed or anticipated that the ring dam 17 has openings to electrically couple the conductive thin film to the electrically conductive patterns. Figure 4A does not show any openings in the ring dam 17 or the cover coat 15. In fact, having openings in the ring dam 17 would prevent the ring dam from performing its intended purpose of preventing the bonding agent from contaminating the bond fingers 12. The Examiner contends that Figure 4A has openings (unlabeled) in the solder mask. However, Figure 4A shows no

openings in the cover coat 15 or the ring dam 17.

Therefore, for the reasons stated above, Applicants believe that the rejections under 35 U.S.C. §102(e) has been overcome. Such action is earnestly solicited.

II. Claims Rejection Under 35 U.S.C. §103(a)

In the Office Action, the Examiner has rejected Claims 1, 8-10, 12, 14, and 17-19 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of Shin, U.S. Patent 6,798,049 and Jones, U.S. Patent 5,639,695. Applicants respectfully disagree with the Examiner's conclusions. Since claim 1 and 14 are both similar in scope, the below arguments apply equally to claim 1 as well as to claim 14.

In claim 1, Applicants claim:

> A semiconductor package, comprising:
> a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof;
> a solder mask formed on the first and second surfaces of the substrate, the solder mask covering the electrically conductive patterns;
> a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;
> a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer;
> an adhesive attached to the second surface of the first semiconductor chip;
> a second semiconductor chip having first and second surfaces, the second surface having a plurality

of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer;

an encapsulate for encapsulating the aperture, the first and second semiconductor chips, and the first and second conductive wires; and

a conductive thin film extending across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

In contrast, Shin discloses an adhesive layer 34 and not a conductive thin film. The adhesive layer disclosed in Shin is used as an insulator. The Examiner claims that an adhesive layer is inherently conductive because it is comprised of matter and that matter inherently conducts physical forces, and electromagnetic, thermal, and sound energy. Applicant respectfully disagrees with this overly broad statement. An insulator by definition is nonconductor of sound, heat or electricity. Shin specifically states in Column 11, lines 45-50, that the adhesive is heat resistant. Thus, Shin does not disclose the adhesive to be thermally conductive.

However, to further distinguish Applicants' claimed invention from the cited prior art, Applicants' conductive thin film extends:

across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the

> solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

In contrast, the adhesive layer 18 in Shin is coupled to the "upper surface of the opening 16 to close the opening 16…" (Column 11, lines 45-46). The Examiner contends that the adhesive layer 18 is coupled "at least indirectly physically" to the solder mask 15 and 17. Applicant is unclear on what the Examiner means by "at least indirectly physically". First, as is clearly shown in Figure 4A, the adhesive layer 18 is not coupled to the cover coat 15. Second, element 17 in Shin is not solder mask. Element 17 is a ring dam. The ring dam 17 is formed on the upper surface of the circuit board to prevent the bonding agent from contaminating the bond fingers 12. Even assuming that the ring dam 17 is a solder mask as claimed by the Examiner, no where in Shin is it disclosed or anticipated that the ring dam 17 is not used for covering the electrically conductive patterns. Furthermore, no where in Shin is it disclosed or anticipated that the ring dam 17 has openings to electrically couple the conductive thin film to the electrically conductive patterns. Figure 4A does not show any openings in the ring dam 17 or the cover coat 15. In fact, having openings in the ring dam 17 would prevent the ring dam from performing its intended purpose of preventing the bonding agent from contaminating the bond fingers

12. The Examiner contends that Figure 4A has openings (unlabeled) in the solder mask. However, Figure 4A shows no openings in the cover coat 15 or the ring dam 17.

On page 10 of the Office Action, the Examiner contradicts his previous statements that Shin discloses a conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask. The Examiner now states that "Shin does not appear to explicitly disclose that the film is electrically coupled; the film absorbs electromagnetic waves and dissipates heat from the first semiconductor device; and wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive film." However, the Examiner now contends that Jones, U.S. Patent 5,639,695 discloses that "electrically conductive patterns 109 formed of the first surface of the resin layer are electrically connected to the conductive film 97, 98." The Examiner further contends that it would have been obvious to combine the electrical connection of Jones with the disclosure in Shin. Applicant respectfully disagrees.

Element 97 in Jones is a heat spreader which is built into the substrate 92. In Figure 4 of Jones, element 97 is not shown to be electrically coupled to the contact pad 109 as stated by the Examiner. Furthermore, nowhere in Jones is it disclosed that

element 97 is electrically coupled to the contact pad 109. With regards to element 98, element 98 is a ground plane layer. The ground plane layer 98 does not extend across the aperture of the substrate and is not coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate. Furthermore, the ground plane layer is not electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

In the Office Action, the Examiner has rejected Claims 2-7, 13, 15 and 16 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of Shin, U.S. Patent 6,798,049 and Jones, U.S. Patent 5,639,695, and further in combination with Fukui, U.S. Patent 6,657,290. Applicants respectfully disagree.

As stated above, neither Shin nor Jones separately or in combination disclose a conductive thin film extending across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask as claimed in claims 1 and 14. Since claims 2-7 and 13 are dependent on claim 1 and claims 15 and 16 are dependent on claim 14, Applicant respectfully submits that these claims are

patentably distinguishable over the cited prior art.

In the Office Action, the Examiner has rejected Claim 11 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the combination of Shin, U.S. Patent 6,798,049 and Jones, U.S. Patent 5,639,695, and further in combination with Lo, U.S. Patent 6,555,902. Applicants respectfully disagree.

As stated above, neither Shin nor Jones separately or in combination disclose a conductive thin film extending across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask as claimed in claims 1 and 14. Since claim 11 is dependent on claim, Applicants respectfully submit that claim 11 is patentably distinguishable over the cited prior art.

Therefore, for the reasons stated above, Applicants believe that the rejections under 35 U.S.C. §103(a) has been overcome. Such action is earnestly solicited.

III. 37 CFR 1.105

In the Office Action, the Examiner reminds the Applicant and the assignee of the requirements under 37 CFR 1.105. The Examiner has asked for patents corresponding to each abstract

listed in the Information Disclosure Statement filed on March 14, 2005. Applicant and the assignee do not have copies of the patents corresponding to each abstract listed in the Information Disclosure Statement filed on March 14, 2005. Applicant and the assignee are only aware of and in possession of the Abstracts which Applicant have already submitted to the Examiner with the Information Disclosure Statement.

IV. Conclusion

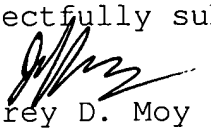
Applicants respectfully submit that Applicants' claimed invention is deserving of patent protection because it describes a useful and functioning apparatus which is patentably distinguishable over the prior art.

In conclusion, Applicants respectfully submit that this Amendment Letter, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1-19 and 27-31 are in condition for allowance. Such action is earnestly solicited.

If the foregoing does not place the case in condition for immediate allowance, the Examiner is respectfully requested to contact the undersigned for purposes of a telephone interview.

If there are any fees incurred by this Amendment Letter, please deduct them from our Deposit Account NO. 23-0830.

Respectfully submitted,



Jeffrey D. Moy
Reg. No. 39,307
Attorney for Applicants

Weiss, Moy & Harris, P.C.
4204 N. Brown Ave.
Scottsdale, AZ 85251
(480) 994-8888 (Phone)
(480) 947-2663 (Fax)

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